REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Objection to Claims 1-40

This objection has been addressed by amending claims 1, 17, and 40 to clarify that the pin signals are both transmitted to *and* received from the target system.

2. Rejection of Claims 1-40 Under 35 USC §102(e) in view of U.S. Patent No. 6,061,511 (Marantz)

This rejection is respectfully traversed on the grounds that the Marantz patent fails to disclose or suggest an emulator and method for probing and monitoring the pin signals of a target interface engine, and in particular one in which:

a. the target system is an actual hardware system; and

b. the pin signals are probed and monitored synchronously with the values of variables of the software algorithm in the processing engine.

Instead, the emulator of Marantz patent *reconstructs* waveforms at each "net" of a design through logic evaluation using saved states of the design. Instead, of monitoring pin signals of a target interface connected to an actual target hardware system, and probing and monitoring the values of variable of processing engine software in synchronism with probing and monitoring of the pin signals, Marantz uses a reconstruction engine to create desired waveforms on the basis of a design netlist and state and input logic traces, and provides them to a user over a user interface. An emulator periodically reports a snapshot of the state elements of the design under emulation to a control program, and the control program, typically running on an engineering workstation interfaced to the emulator, controls the emulation.

In addition, the Marantz patent fails to disclose or suggest a system level mechanism for the emulator to monitor and buffer the pin signals and variables, or a method for

detecting triggering events under execution of the processing engine by inserting in advance software routines into the software algorithm to automatically invoke an interrupt mechanism during the emulation, as recited in various dependent claims.

The present invention is directed to an emulator for verifying the logic design of a target chip to mounted in a target system. The target system is an actual hardware system, which performs a specific operation, while the emulator includes both a processing engine and a target interface engine. The processing engine is made of hardware components and executes a software algorithm corresponding to the logic design of the target chip, while the software algorithm is down loaded from a workstation to the processing engine, and the target interface engine is also made of hardware components and interfaces with the target system in response to the execution of the software algorithm by the processing engine. By providing both a processing engine that monitors software variables of the software algorithm and tracks time-varying changes in the software variables, and a target interface engine that monitors hardware pin signals and tracks time-varying changes in the hardware pin signals under the control of the processing engine, monitoring of the timings of the hardware pin signals and the software variables can be synchronized.

The Marantz patent is not concerned with being able to monitor hardware pin signals and software algorithm execution (via changes in software variables) in a synchronized manner, as claimed. The field of application of the system of Marantz relates to the logic design stage in which an FPGA-based emulation and an evaluation method are used. This stage does not correspond to that of the claimed invention, which concerns verification of chip logic at the algorithm stge, and especially for verifying chip logic under a target system environment. Marantz is instead concerned with the final logic design and verifying stage, and in particular with economic use of verification resources. To achieve this end, the Marantz patent discloses a system and method of reconstructing waveforms during the logic evaluation stage in order to debug specified "nets" during a specified time frame using statuses and signal information that were saved in advance during the modeling stage of the

chip design. **This has nothing to do with either the objectives or the implementation of the claimed invention, and is not suggestive of the claimed synchronized monitoring and debugging the variable in the software implementing the emulation mechanism and the pin signals of the target system hardware.**

Because the Marantz patent does not disclose all elements recited in claims 1-40, withdrawal of the rejection under 35 USC §102(e) is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, withdrawal of the rejections and expedited passage of the application to issue is requested.

Respectfully submitted,

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